REMARKS

Claims 41-50 are currently present in this application. In view of the remarks that follow, reconsideration is respectfully requested.

Compliance With 35 U.S.C. §132

Applicants' last Response amended only the claims. At the top of page 2, the present Office Action objects to those claim amendments under 35 U.S.C. §132, asserting that the claim amendments introduce new matter into the disclosure of the invention. This ground of objection is respectfully traversed, because it is not a proper ground of objection. More specifically, as noted above, Applicants last Response amended only the claims. MPEP §2163.01 and §706.03(o) make it clear that an amendment to a claim should never result in a rejection under 35 USC §132 on the ground that "new matter" has been added to the disclosure. The rejection, if any, should be a 35 U.S.C. §112 rejection on the ground that the amended claim includes subject matter that is not supported by the originally-filed disclosure. (The present Office Action contains a rejection under §112, which is discussed below).

As explained above, the objection under §132 is not proper, because it is a type of objection prohibited by the PTO. It is therefore respectfully submitted that this ground of objection must be withdrawn, and Applicants respectfully request notice that this ground of objection has been withdrawn.

Compliance With 35 U.S.C. §112 - First Paragraph

The Office Action rejects Claims 41-50 under the first paragraph of 35 U.S.C. §112, asserting that the claims recite subject matter for which the specification fails to provide a written description. This ground of rejection is respectfully traversed, for the following reasons.

The Office Action asserts that the specification fails to provide a written description of the claim limitations of "a first set of logic devices" and "a second set of logic devices".

Applicants respectfully disagree. The specification clearly indicates at a number of locations that the disclosed structure includes multiple logic devices, for example in paragraph [0012], paragraph [0018], and paragraph [0023]. Further, the specification clearly recognizes that one subset of these plural logic devices may differ from another subset thereof. For example, paragraph [0024] refers to "selected logic devices", which necessarily means that the "selected logic devices" can constitute one subset of the plural logic devices, and that the non-selected logic devices inherently constitute a second subset of the plural logic devices. Applicants' specification does not use the exact phrases "a first set of logic devices" and "a second set of logic devices". However, as pointed out in MPEP §2173.05(e), the terminology used in the claims does not have to exactly match the terminology used in the specification. It is therefore respectfully submitted that it is perfectly proper for Applicants' claims to refer to two subsets of plural logic devices, for example as "a first set of logic devices" and "a second set of logic devices".

The Office Action also asserts that the specification fails to provide a written description of the claim limitations of "an operating voltage" for the first set of logic devices and "an operating voltage" for the second set of logic devices". Persons skilled in the art are thoroughly familiar with the fact that logic devices necessarily and inherently have operating voltages. Moreover, Applicants' specification expressly refers to the operating voltages of the logic devices, for example in paragraph [0004]. To the extent the specification also recognizes that the logic devices can include two or more subsets, as discussed above, persons skilled in the art will readily understand that the logic devices in each set will necessarily have an operating voltage. Accordingly, it is perfectly proper for Applicants' claims to refer to "an operating voltage" for one set of logic devices and "an operating voltage" for another set of logic devices.

In view of the foregoing, it is not at all clear why the Office Action asserts that there is no written description corresponding to the recitation of two sets of logic devices, or the recitation that logic devices have operating voltages. It is respectfully submitted that the originally-filed

specification does in fact provide a written description that properly supports all of the claim language in question, and notice to that effect is respectfully requested.

Independent Claim 41

Independent Claim 41 stands rejected under 35 U.S.C. §103 on the ground that it would be obvious over Choi U.S. Patent No. 6,894,356, taken in view of Chidambarrao U.S. Patent No. 6,709,926. This ground of rejection is respectfully traversed. MPEP §2142 specifies that:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

Applicants respectfully submit that Choi and Chidambarrao fail to establish a prima facie case of obviousness under §103 with respect to Claim 41, because the proposed modification to Choi would not result in the combination that is recited in Applicants' Claim 41. In more detail, Applicants initially note that Choi appears to disclose the use of only a low-k dielectric material, and not any high-k dielectric material. Conversely, Chidambarrao appears to disclose the use of only a high-k dielectric material, and not any low-k dielectric material.

In explaining the §103 rejection of Claim 41, the Office Action begins by indicating that Choi discloses an integrated circuit (IC) with memory devices and logic devices that all have a non-high-k gate dielectric, but Choi fails to disclose any logic devices with a high-k gate dielectric. The Office Action then turns to Chidambarrao, noting that Chidambarrao mentions a logic transistor with a high-k gate dielectric and with high-speed performance. The Office Action asserts that it would be obvious to modify the logic devices disclosed in Choi by replacing the non-high-k gate dielectric with a high-k gate dielectric, in order to obtain high-speed performance in Choi's logic devices. But even assuming for the sake of discussion that a

person of ordinary skill in the art would actually be motivated to make the proposed modification, the stated motivation would cause that person to modify **all** of the logic devices in Choi so that they would **all** enjoy high-speed performance. In other words, the Office Action does not take the position that a person of ordinary skill would modify some but not all of the logic devices in Choi, and in particular does not offer any rationale as to why a person of ordinary skill would be motivated to modify some but not all of the logic devices, especially since the asserted motivation for the modification is to obtain improved performance. Consequently, the **modified** Choi IC would have all of its memory devices implemented with a non-high-k gate dielectric, **all** of its logic devices implemented with a high-k gate dielectric, and **no** logic devices implemented with a non-high-k gate dielectric. Thus, the modified Choi IC would **not** have any devices corresponding to the limitation in Claim 41 of "a second set of logic devices having a non-high-k gate dielectric". Accordingly, it is respectfully submitted that the proposed modification to Choi would not result in the specific combination that is recited in Applicants' Claim 41. It is therefore respectfully submitted that that the Office Action fails to establish a prima facie case of obviousness under §103 with respect to Claim 41. Claim 41 is therefore believed to be patentably distinct from Choi and Chidambarrao, and notice to that effect is respectfully requested.

Independent Claim 45

Independent Claim 45 stands rejected under 35 U.S.C. §103 on the ground that it would be obvious over Choi in view of Chidambarrao. This ground of rejection is respectfully traversed. As noted earlier, the PTO specifies in MPEP §2142 that:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

Applicants respectfully submit that Choi and Chidambarrao fail to establish a prima facie case of obviousness under §103 with respect to Claim 45, because the proposed modification to Choi would not result in the combination recited in Applicants' Claim 45. As noted above, Choi appears to disclose the use of only a low-k dielectric material, and no high-k dielectric material. Chidambarrao appears to disclose the use of only a high-k dielectric material, and no low-k dielectric material.

In explaining the §103 rejection of Claim 45, the Office Action begins by proposing the same modification that was proposed in association with Claim 41, namely replacing the non-high-k gate dielectric in the logic devices of Choi with a high-k gate dielectric. However, as discussed above in association with Claim 41, the result would be that all logic devices of Choi would be modified and have a high-k gate dielectric.

The explanation of the §103 rejection of Claim 45 also proposes a second modification to Choi. In particular, the Office Action proposes that, since Chidambarrao has memory devices with a high-k dielectric, it would be obvious to modify the memory devices disclosed in Choi by replacing the non-high-k dielectric with a high-k dielectric. However, the Office Action fails to offer any motivation for making this proposed modification. As explained in MPEP §706.02(j):

> 35 U.S.C. 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. After indicating that the rejection is under 35 U.S.C. 103, the examiner should set forth in the Office action:
>
> :
>
> (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification.

Since the present Office Action fails to offer any motivation as to why a person of ordinary skill might possibly be motivated to make the proposed modification to memory devices in Choi, the Office Action fails to satisfy one of the fundamental requirements for establishing a prima facie case of obviousness under §103. Absent motivation, a person of ordinary skill would not make the proposed modification to the **memory** devices of Choi. And even assuming for the sake of discussion that a person of ordinary skill would actually be motivated to make the proposed modification to the **logic** devices, the stated motivation for that modification would cause the person to modify **all** of the logic devices in Choi so that they would **all** enjoy high-speed performance. Consequently, the **modified** Choi IC would have all of its memory devices implemented with a non-high-k gate dielectric, **all** of its logic devices implemented with a high-k gate dielectric, and **no** logic devices implemented with a non-high-k gate dielectric. Thus, after modification, the Choi IC would **not** have any device corresponding to either the limitation in Claim 45 of "a second set of logic devices having a non-high-k gate dielectric", or the limitation in Claim 45 of "a set of memory devices having a high-k gate dielectric".

It is therefore respectfully submitted that the proposed modification to Choi would not result in the specific combination that is recited in Applicants' Claim 45. Accordingly, it is respectfully submitted that that the Office Action fails to establish a prima facie case of obviousness under §103 with respect to Claim 45, and that Claim 45 is therefore patentably distinct from Choi and Chidambarrao. Notice to that effect is respectfully requested.

Independent Claim 48

Independent Claim 48 stands rejected under 35 U.S.C. §103 on the ground that it would be obvious over Choi in view of Chidambarrao. This ground of rejection is respectfully traversed. As noted earlier, the PTO specifies in MPEP §2142 that:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not

produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

Applicants respectfully submit that Choi and Chidambarrao fail to establish a prima facie case of obviousness under §103 with respect to Claim 48, because the proposed modification to Choi would not result in the combination recited in Applicants' Claim 48. As noted above, Choi appears to disclose the use of only a low-k dielectric material, and no high-k dielectric material. Chidambarrao appears to disclose the use of only a high-k dielectric material, and no low-k dielectric material.

In explaining the §103 rejection of Claim 48, the Office Action begins by proposing the same modification that was proposed in association with Claim 41, namely replacing the non-high-k gate dielectric in the logic devices of Choi with a high-k gate dielectric material. However, as explained above in association with Claim 41, the result would be that all logic devices of Choi would be modified to have a high-k gate dielectric. Further, it is not clear why the Examiner proposes this particular modification in the case of Claim 48, because Claim 48 does not happen to recite any logic devices that have a high-k gate dielectric. Instead, Claim 48 recites two sets of logic devices that have different non-high-k gate dielectrics.

Next, the Office Action proposes the same modification that was proposed in association with Claim 45, namely modifying all of the memory devices of Choi to replace the non-high-k gate dielectric with a high-k gate dielectric. However, as explained above in association with Claim 45, the Office Action fails to offer any motivation for this proposed modification. Absent motivation, a person of ordinary skill would not make the proposed modification to any of the memory devices in Choi. Consequently, in the absence of any stated motivation, the Office Action has failed to meet the requirements of MPEP §706.02(j) in regard to establishing a prima facie case of obviousness.

Finally, and still in regard to Claim 48, the Examiner proposes a third modification to Choi. However, the Office Action fails to clearly identify what this proposed modification would

be. In particular, in the last line on page 4, the Office Action includes a statement that "Chidambarrao et al. also disclose", but then in lines 1-2 on page 5, the Office Action fails to actually identify what it is that Chidambarrao supposedly discloses. Instead, the Office Action refers to Choi instead of Chidambarrao. In particular, the Office Action refers to the gate dielectric 308 shown in Figure 4A of Choi, and refers to lines 1-5 in column 6 of Choi. In other words, the Office Action proposes that Choi be modified in view of itself, which does not make sense. Modifying Choi in view of itself effectively means no modification at all.

In summary, and assuming for the sake of discussion that a person of ordinary skill would actually be motivated to make the first proposed modification to Choi, the stated motivation would cause that person to modify all of the logic devices in Choi so that they would all enjoy high-speed performance. As to the second proposed modification, the Office Action offers no motivation, and so a person of ordinary skill simply would not make the second proposed modification at all. And as to the third proposed modification, the Office Action winds up proposing that Choi be modified in view of itself, which does not make any sense, and which effectively boils down to no modification. Consequently, taking all three proposals into account, the modified Choi IC would have all of its memory devices implemented with a non-high-k gate dielectric, all of its logic devices implemented with a high-k gate dielectric, and no logic devices implemented with a non-high-k gate dielectric. Thus, the modified Choi IC would not have any devices corresponding to any of the following limitations of Claim 48:

> a first set of logic devices having a first non-high-k gate dielectric;
>
> a second set of logic devices having a second non-high-k gate dielectric different from said first non-high-k gate dielectric; and
>
> a set of memory devices having a high-k gate dielectric.

It is therefore respectfully submitted that the proposed modification to Choi would not yield an IC that is even remotely similar to the specific combination recited in Applicants' Claim 48. It is therefore respectfully submitted that that the Office Action fails to establish a prima facie case of obviousness under §103 with respect to Claim 48, and that Claim 48 is thus patentably distinct from Choi and Chidambarrao. Notice to that effect is respectfully requested.

Dependent Claims 42-44, 46-47 and 49-50

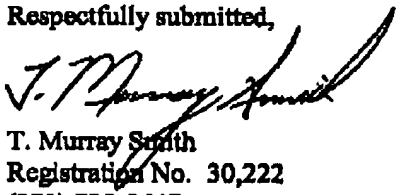
Claims 42-44, Claims 46-47 and Claims 49-50 respectively depend from Claim 41, Claim 45 and Claim 48, and are also believed to be distinct from the art of record, for example for the same reasons set forth above with respect to Claims 41, 45 and 48, respectively.

Conclusion

Based on the foregoing, it is respectfully submitted that all of the pending claims are fully allowable, and favorable reconsideration of this application is therefore respectfully requested. If

the Examiner believes that examination of the present application may be advanced in any way by a telephone conference, the Examiner is invited to telephone the undersigned attorney at 972-739-8647.

Respectfully submitted,



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Enclosures: None

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